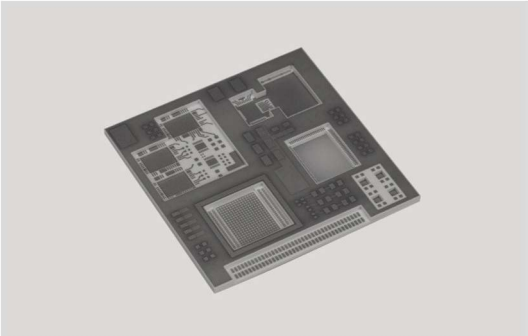
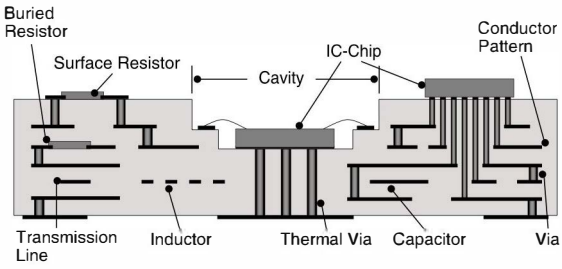
EU RoHS COMPLIANT



construction



ordering information

New Part #

KLC	AB1
Type	KOA Ref. Number

features

- Suitable for bare chip mounting as it has thermal expansion coefficient close to that of silicon and excellent dimensional accuracy and flatness.
- Excellent high frequency characteristics are achieved by the low-loss dielectric ceramic and the low-loss conductor.
- Downsizing and high integration density can be achieved by the multilayer wiring, the multi-cavity structure and the surface/buried resistor printing.
- The substrate and the cavity can be formed in round, polygonal, concave or convex shape.
- Thermal vias can be placed in the bare chip mounting area to improve the thermal conductivity of the substrate.
- The use of ceramic material contribute to the excellent heat and humidity resistance and prevents outgas and dust generation.
- Products meet EU RoHS requirements

what is LTCC ?

LTCC stands for Low Temperature Co-fired Ceramics.

LTCCs are multilayer ceramic substrates that can be fired simultaneously with low-resistance conductors since the glass-based material is added to the alumina material to lower the firing temperature compared to the general ceramic firing process.

On KOA's LTCC, silver (Ag) based paste that has low conductor resistance is co-fired to create the conductor patterns on each layer of the ceramic substrate.

It realizes the multilayer substrate with excellent low-loss electrical characteristics as well as high dimensional accuracy.

KOA's LTCC also provides downsizing by integrating resistors and transmission lines in the inner and surface layers of the substrate. In addition, the thermal expansion coefficient close to silicon enhances the reliability of the bare chip mounting, and the cavity structure contributes to the lower profile package.

high-precision specification

Substrates with higher precision based on the LTCC multilayer substrate are available.

- High-precision pad positioning and excellent flatness.
- High-density wiring structure by utilizing LTCC multilayer substrate.

Please contact us for details.

environmental applications

Characteristics of Substrate Material

Parameter	Characteristics
Bending Strength (MPa)	250
Thermal Expansion Coefficient (x10^{-6}/K)	5.5
Thermal Conductivity (W/m • K)	3
Insulation Resistance (Ω • cm)	>10^{13}
Dielectric Constant at 1GHz	6.6
Dielectric Loss at 1GHz	0.004
Density (g/cm^3)	2.8
Surface Roughness Ra (μm)	<0.4
Withstanding Voltage (kV/mm)	>15
Substrate Thickness (mm)	0.4~2.0 Standard
Layer Thickness (μm/Layer)	80, 100, 125 Standard

Standard Design Rules

Symbol	Parameter	Design Value
A	Line Width	0.06mm Min.
B	Line to Line Spacing	0.06mm Min.
C	Via Diameter	0.1mm, 0.15mm, 0.2mm
D	Via Pad Diameter	Via diameter +0.05mm Min.
E	Via to Via Spacing	0.2mm Min.
F	Via pad to Line Spacing	0.125mm Min.
G	Part Edge to Conductor Spacing	0.2mm Min.
H	Part Edge to Via Spacing	0.3mm Min.
J1, J2	Cavity Width	0.6mm Min.
K1, K2	Cavity Depth	0.1mm Min.
L	Wall Width of Cavity	0.5mm Min.
M	Shelf Width in the Cavity	0.5mm Min.

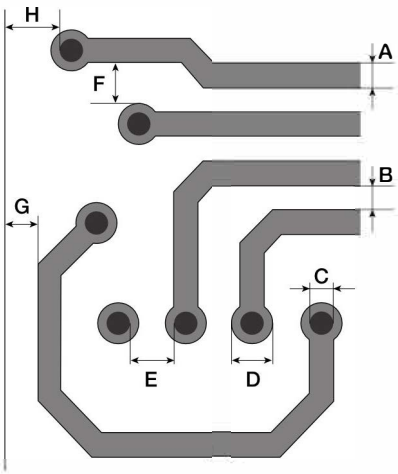
Conductor

Parameter	Characteristics
Material of Conductor	Ag
Resistivity of Conductor (μΩ • cm)	2.5
Surface Plating	Ni-Au, Ni-Pd-Au

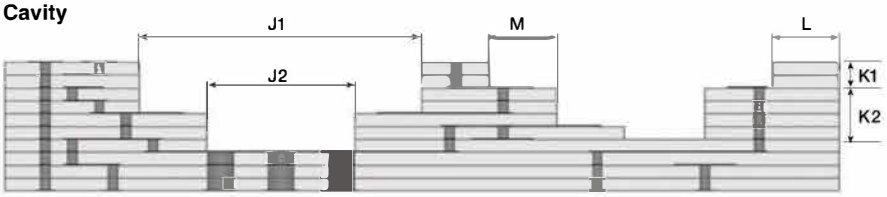
Surface/Buried Printed Resistor

Parameter	Surface Resistor	Buried Resistor
Resistance Range (Ω)	10 ~ 100k	10 ~ 200k
Resistance Tolerance (%)	±5	±20 ~ 50

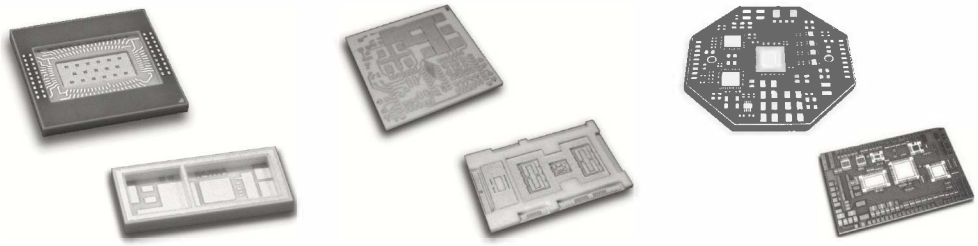
Surface layer - Inner layer



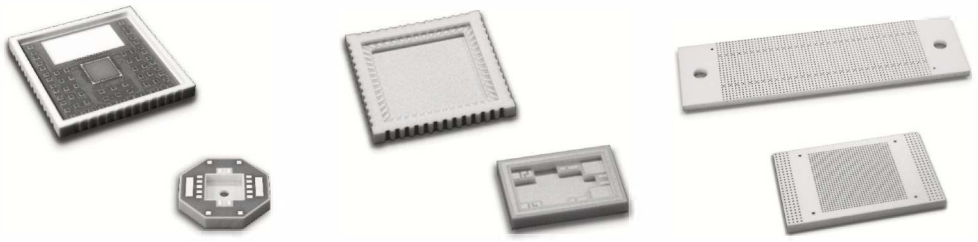
Cavity



* Please contact us for the use out of the standard design rules, and detailed design rules.



Sensor Module | RF Module | Multi Chip Module



MEMS Sensor Package | Various Device Package | Interposer Substrate